REMARKS

The Office Action of November 28, 2005 was received and its content has been reviewed. The Examiner is thanked for reviewing this application and withdrawing finality of the previous Office Action.

Claims 1-5 and 21-29 are pending for consideration, and claims 6-20 have previously been withdrawn from consideration.

Referring now to the detailed Office Action, claims 1, 3-5, 21, 23-26, 28 and 29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over admitted prior art ("Admission") in view of McGibney et al. (U.S. Patent No. 6,112,322 – hereafter McGibney) and McClure (U.S. Patent No. 6,037,792 – hereafter McClure). Further, claims 2, 22 and 27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over admitted prior art ("Admission") in view of McGibney and McClure, and further in view of Fontana et al. (U.S. Patent No. 5,982,677 – hereafter Fontana). These rejections are respectfully traversed at least for the reasons provided below.

Initially, the Examiner is thanked for acknowledging that Applicant's arguments with respect to the rejection of claims 1, 21 and 26 and in relation to the selection of all word lines by the row decoder submitted in the Request for Reconsideration filed November 7, 205 were persuasive. However, despite the Examiner's acknowledgement that Applicant's arguments were persuasive, the Examiner repeated substantially the same erroneous assertion in the §103(a) rejection of claims 1, 3-5, 21, 23-26 and 28-29. Particularly, in applying Admission in the rejection, the only difference in the Examiner's prior assertion and the current assertion is that Admission is not clear that the row decoder is connected to the test mode circuit and applies the excess voltage to all the word lines. That is, the Examiner simply alleged that Admission teaches a row decoder but not a row decoder connected to the test mode circuit. Further, the Examiner continued to assert that a test mode circuit for outputting a test mode signal was disclosed in implied situation, for example, to control the selection of all word line.

Again, in response to the Examiner's assertions, Applicant respectfully submits that the Examiner's assertions are clearly incorrect. Contrary to the Examiner's incorrect assertion, in the background section of the present specification, it is disclosed that the test mode circuit applies the test mode voltage to all word lines. There is no description or

implication that the test mode circuit controls the selection of all word line.

Moreover, in the Examiner's assertion that "a column decoder with column switches are inherent in the memory of admission", Applicant respectfully submits that the Examiner's assertion is incorrect, as the column decoder and the column switches are completely different. For example, Fig. 1 of U.S. Patent No. 6,791,882 ('882 teaching reference, which is a teaching reference, shows a column decoder (YDCR) and column switches Q7 to Q9 as separate and distinct independent elements. There is nothing in Admission or the exemplary '882 teaching reference of a column decoder with column switches being inherent in a memory device.

With respect to McClure, as submitted previously, the reference discloses a semiconductor memory device having a flag terminal for outputting a burn-in stress test signal. The burn-in stress test of McClure is different from the oxide film stress test of the present invention, as previously submitted in the Request for Reconsideration filed November 7, 2005. Moreover, since the test mode circuit disclosed in McClure is not connected to the column decoder and the row decoder, the test mode circuit of McClure is completely different from the presently claimed invention.

With respect to McGibney, the reference teaches that a group of one or more word lines are selected (see column 2, lines 11-12). Further, col. 2, lines 48-52 of McGibney states the following:

> *The invention provides a circuit and method for incrementally selecting and deselecting word lines, thereby enabling the performance of stress tests in EEPROMs without the power surge that would result from simultaneously switching all word lines in the EEPROM memory array. A method is provided for selecting and deselecting word lines in groups of one or more, on receipt of a single initiating signal.* (emphasis added)

That is, to avoid power surge, McGibney teaches that an excess voltage is not applied to all word lines, but to some, incrementally in groups.

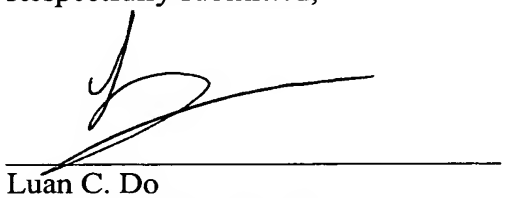
The requirements for establishing a *prima facie* case of obviousness, as detailed in MPEP §2143 - 2143.03 (pages 2100-122 - 2100-136), are: first, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference to combine the teachings; second, there must be a reasonable expectation of success; and, finally, the prior art reference

(or references when combined) must teach or suggest all of the claim limitations. As Admission, McClure and McGibney are deficient as discussed above, and as there is no motivation or suggestion in the cited prior art references to combine their respective different teachings to arrive at Applicant's claimed invention, their combination in the obviousness rejections are improper and a *prima facie* case of obviousness has not been established.

The arguments set forth above with respect to the Admission, McClure and McGibney in the rejection of claims 1, 3-5, 21, 23-26 and 28-29 are also applicable to the rejection of claims 2, 22 and 27, as Fontana does nothing to cure the above-discussed deficiencies of Admission, McClure and McGibney.

In view of the foregoing, it is respectfully requested that the rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-5 and 21-29 be allowed and that the application be passed to issue. If a conference would expedite prosecution of the instant application, the Examiner is hereby invited to telephone the undersigned to arrange such a conference.

Respectfully submitted,



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